LS8T41505

V1.2

2024 09

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(Tel) 025-58600707

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	˜	V1.2
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˜	˜	ṗ
1	V1.0	ṗ
2	V1.03	Δ Ǔ
3	V1.04	– ϶ Ʉ ₣ ḱ ϶ ⁝⁝ 1
4	V1.1	Ʉ ƀ ǐ ч -40 +105 ⁝⁝ 1 Ţ VDDOO ḱ ч 1.8V 3.3V ᴸ XIN ˜ ч 1.8V ɲ ѵ 2 Ţ θ J꜀ ч 42 /W 3VDDOO ⍱ ỵ 1.8V ´E 4 Ţ ɾ ą ⁝,⁝ ⌠ PLL ŋ 5 ѵ OUTOB □ β Ⅵ ₩ Ḥ
5	V1.2	ḱ ₩ ṗ Ʉ ESD Ḥ ⌠ ض ⁝⁝ 13 14 36 39 40 ϶ ḱ ض ⊓ ϶ ᴇ 2 ĩ ق ɲ ḱ ϶ 3 ˜ ỵ ≠ ϶ W ᴇ ŋ ϶,⁝ ᴇ Ⅵ ₩ Ḥ Ţ ḱ ϶ LS8T41505 ƀ ᴍ Ⅵ Ʉ ѵ Ð A ᴇ ч 245 ; Ð B PCB

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ڤU ⊢ service@loongson.cn

1.

LS8T41505 25MHz r ~ o ₣ `l LVDS LVCMOS ¿ LPHCSL

Ь □ ₣ ☋ ì Ţ LVCMOS ˆ D 100MHz Ḥˆ LVDS

ˆ D 200MHz Ḥˆ LPHCSL ˆ D 100MHz Ḥˆ hˆ

˜ ˆ L 4 ₣ Ь □ ˙˙ ˆ

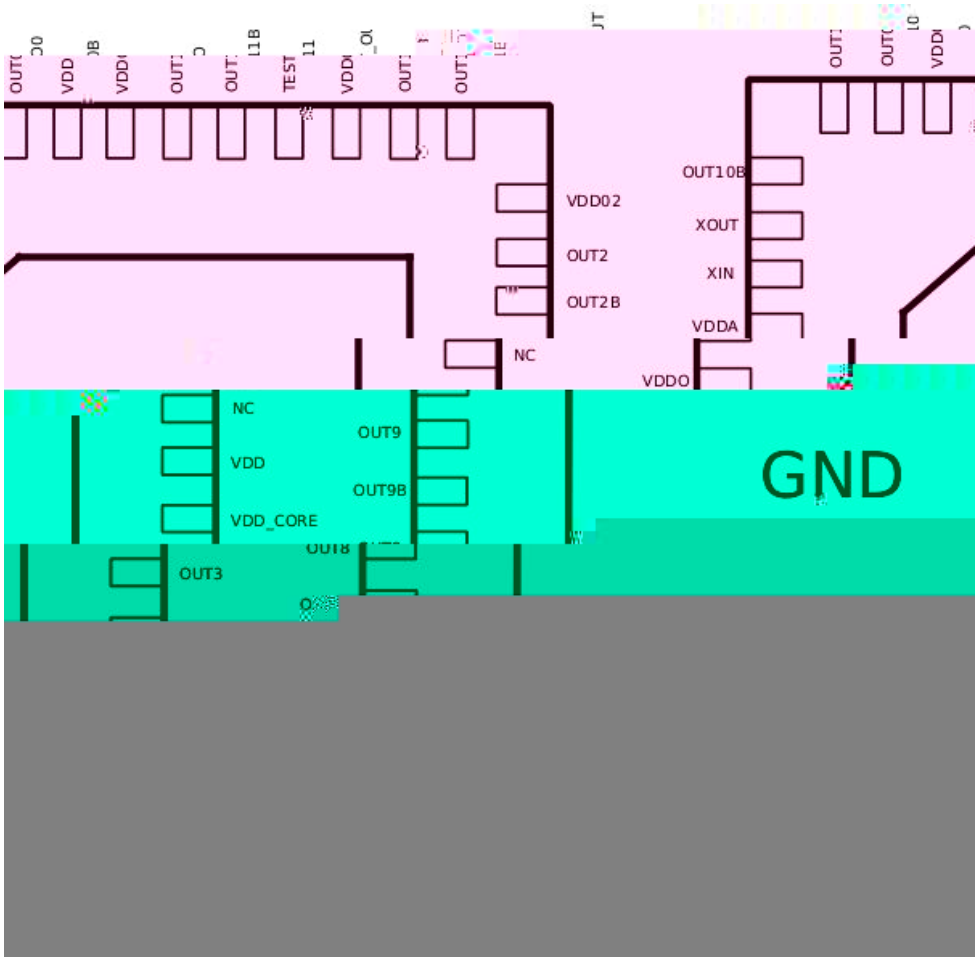
G PC ĭ h PCIE2.0

2. ℠ ☪

- ~ ㄱ ч 3.3V 1.8V
- `l LVCMOS LPHCSL ¿ LVDS ‰ ₣
- ₣
  - OUT0 25MHz/100MHz LVCMOS
  - OUT1 33.33MHz LVCMOS/100MHz LP-HCSL/25MHz LP-HCSL
  - OUT2 100MHz LVCMOS/100MHz LP-HCSL/200MHz LVDS/156.25MHz LP-HCSL
  - OUT3 5-11 100MHz LP-HCSL
  - OUT4 100MHz/200MHz LVDS/100MHz LP-HCSL
- 25MHz r ъ ч ~ ă
- ъ -40 +105

3. ₣ ↓ ㄋ

ㄋ 1 ч LS8T41505 ↓ ㄋ 1 ч LS8T41505



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O	Ḥ O	~ ₹	w
1	OUT10B	Output	Output Clock10 ǐ ₹ 100MHz LP-HCSL Ḥ
2	XOUT	Input	r ᶊ o ₹
3	XIN/REF	Input	25MHz r ᶊ ϒ 25MHz ‰ o ~ 1.8V
4	VDDA	Power	w 1.80V
5	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
6	OUT9	Output	Output Clock9 ₹ 100MHz LP-HCSL Ḥ
7	OUT9B	Output	Output Clock9 ǐ ₹ 100MHz LP-HCSL Ḥ
8	OUT8	Output	Output Clock8 ₹ 100MHz LP-HCSL Ḥ
9	OUT8B	Output	Output Clock8 ǐ ₹ 100MHz LP-HCSL Ḥ
10	OUT7	Output	Output Clock7 ₹ 100MHz LP-HCSL Ḥ
11	OUT7B	Output	Output Clock7 ǐ ₹ 100MHz LP-HCSL Ḥ
12	OE	Input	₹ ą ϒ
13	SEL1	Input	₹ 5 ṗ ⁘
14	SEL0	Input	₹ 5 ṗ ⁘
15	VDD	Power	1.80V
16	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
17	OUT6	Output	Output Clock6 ₹ 100MHz LP-HCSL Ḥ

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18	OUT6B	Output	Output Clock6 ḭ ₹ 100MHz LP-HCSL Ḥ
19	OUT5	Output	Output Clock5 ₹ 100MHz LP-HCSL Ḥ
20	OUT5B	Output	Output Clock5 ḭ ₹ 100MHz LP-HCSL Ḥ
21	VDDO4	Power	OUT4 3.30V
22	OUT4	Output	Output Clock4 ₹ 100MHz LP-HCSL 100MHz/200MHz LVDS Ḥ
23	OUT4B	Output	Output Clock4 ḭ ₹ 100MHz LP-HCSL 100MHz/200MHz LVDS Ḥ
24	NC	NC	
25	NC	NC	ΓΛ
26	NC	NC	
27	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
28	OUT3B	Output	Output Clock3 ḭ ₹ 100MHz LP-HCSL Ḥ
29	OUT3	Output	Output Clock3 ₹ 100MHz LP-HCSL Ḥ
30	VDD_Core	Power	VCO ㄱ ㄴ 1.80V
31	VDD	Power	1.80V
32	NC	NC	
33	NC	NC	
34	OUT2B	Output	Output Clock2 ḭ ₹ 100MHz LVCMOS 100MHz LP-HCSL 200MHz LVDS Ḥ 156.25MHz LP-HCSL Ḥ
35	OUT2	Output	Output Clock2 ₹ 100MHz LVCMOS 100MHz LP-HCSL 200MHz LVDS Ḥ 156.25MHz LP-HCSL Ḥ
36	VDDO2	Power	OUT2/OUT2B PLL ㄴ 3.30V
37	OUT1B	Output	Output Clock1 ḭ ₹ 33.33MHz LVCMOS ㅋ □ β ₹ 100MHz LP-HCSL 25MHz LP-HCSL № Ḥ
38	OUT1	Output	Output Clock1 ₹ 33.33MHz LVCMOS 100MHz LP-HCSL 25MHz LP-HCSL Ḥ
39	VDDO1	Power	OUT1/OUT1B OSC 3.30V
40	TEST_OUT	Output	Ḥ o β
41	OUT11	Output	Output Clock11 ₹ 100MHz LP-HCSL Ḥ
42	OUT11B	Output	Output Clock11 ḭ ₹ 100MHz LP-HCSL Ḥ
43	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
44	VDD	Power	1.80V
45	OUT0B	Output	Output Clock0B ₹ 25MHz/100MHz LVCMOS □ β Ḥ
46	VDDO0	Power	OUT0/OUT0B 1.80V 3.30V
47	OUT0	Output	

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LS8T41505 CPU h 7A1000 7A2000 ą

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45	OUTOB	LVCMOS	30		45	5		20	
47	OUTO	LVCMOS	20		40	10		30	
37,38	OUT1/	LVCMOS	20		30	20	24	30	
	OUT1B	LP-HCSL	13		19	31	33	37	
34,35	OUT2/	LVCMOS	20		30	20	24	30	

		LP-HCSL	13		19	31	33	37	
		LVDS	70		90	10		30	
28,29	OUT3/ OUT3B	LP-HCSL	13		19	31	33	37	
22,23	OUT4/ OUT4B	LP-HCSL	13		19	31	33	37	
		LVDS	70		90	10		30	
19,20,17,18,10,11,8,9,6,7,1,48,41,42	OUT5-OUT11 /OUT5B-OUT 11B	LP-HCSL	13		19	31	33	37	

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3 Н˜ ч □ L ї ⁞ ⁚

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4 OUT1 є OUT1B OUT2 є OUT2B OUT3 є OUT3B OUT4 є OUT4B OUT5 є OUT5B OUT6 є OUT6B OUT7 є OUT7B OUT8 є OUT8B OUT9 є OUT9B OUT10 є OUT10B OUT11 є OUT11B ч № Н˜

5 epad ˆ ѵ PCB ѕ

5. ѵ Ь ƀ Ð

ѵ Й

2 ѵ

≠ VDD	0V 2.7V
ṗ ≠ VDD_CORE	0V 2.7V
≠ VDDA	0V 2.7V
₮ ⌟ ˪ ≠ VDDO	0V 2.7V
₮ ⌟ ˪ ≠ VDDO0	0V 5.0V
₮ ⌟ ˪ ≠ VDDO1	0V 5.0V
₮ ⌟ ˪ ≠ VDDO2	0V 5.0V
₮ ⌟ ˪ ≠ VDDO4	0V 5.0V
	-65 150
ƀ	200mA
θ J_c	42 /W
ESD HBM	1000V

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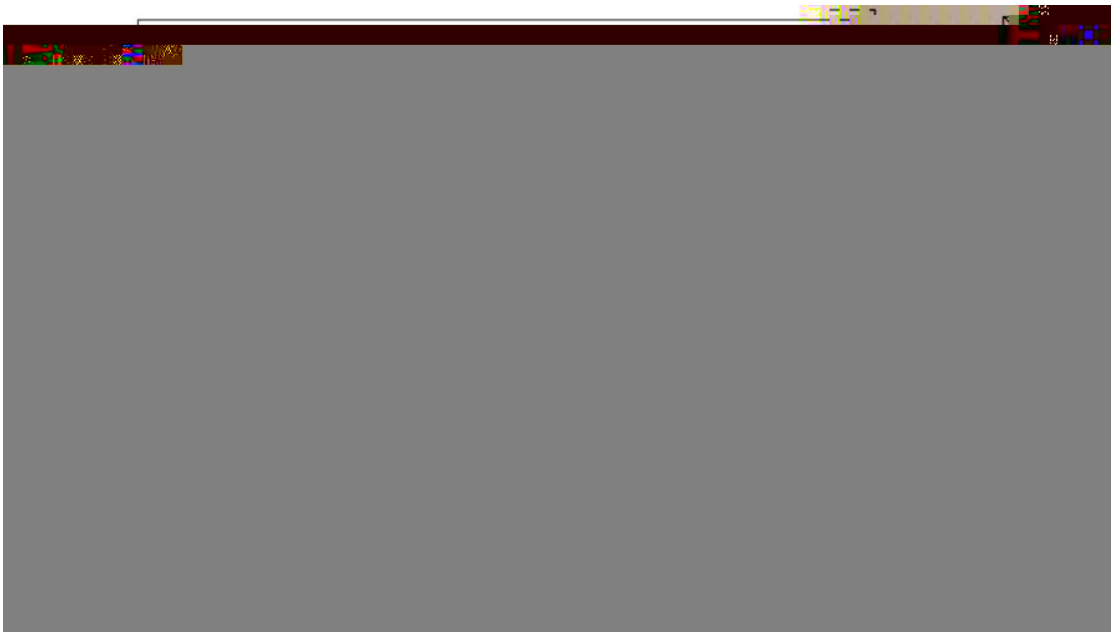
3 ƀ Ð

≠ VDD	1.8V ± 5%
ṗ ≠ VDD_CORE	1.8V ± 5%

ㄴ VDDA	1.8V ± 5%
ㅔ ㄱ ㄴ ㄴ VDDO	1.8V ± 5%
ㅔ ㄱ ㄴ ㄴ VDDO0	1.8V ± 5%　3.3V ± 5%
ㅔ ㄱ ㄴ ㄴ VDDO1	3.3V ± 5%
ㅔ ㄱ ㄴ ㄴ VDDO2	3.3V ± 5%
ㅔ ㄱ ㄴ ㄴ VDDO4	3.3V ± 5%
~	25MHz ± 20ppm
ㅂ	-40

LVDS			
LVDS ẏ	V_{OT}		240
LVDS ẏ ĩ.	ΔV_{OD}		
LVDS ˜	V_{OS}	VDDO0=VDDO1=VDDO2=VDDO4=3.3V,VD	1.12
LVDS ˜ ĩ.	ΔV_{OS}	DO=VDDA=VDD_CORE=VDD=1.8V	
LVDS ˜	I_{OS}		
LVDS ˜ ĩ.	I_{OSD}		
LP-HCSL			
LPHCSL	V_{OH}	VDDO0=VDDO1=VDDO2=VDDO4=3.3V,VD	0.60
LPHCSL ˙	V_{OL}	DO=VDDA=VDD_CORE=VDD=1.8V	-0.15
⁘ ˀ / Ӣ	t_R / t_F	VDDO0=VDDO1=VDDO2=VDDO4=3.3V,VD DO=VDDA=VDD_CORE=VDD=1.8V	1
ˀ	t_{RF}		0.22
˜	f_{IN}		
₹	f_{OUT}		25
VCO	f_{VCO}	VCO ƀ ॐ	
☋	f_{PFD}	☋ ƀ	
	f_{BW}	˜ Ч 25MHz	0.05
˜ ∖	t_2		45
₹ ∖	t_3		40
ˀ	t_4	3.3V LVCMOS ₹ ⁘ ˀ =5pF	1.2
⁘ ˀ / Ӣ	t_5	LVDS	0.5
jitter	t_6	RMS β jitter ă OUT0 25MHz LVCMOS ₹	0.5
		RMS β jitter № ₹ 100MHz LP-HCSL ₹	
	t_7	ɾ ⁘ ⌡ PLL	
		ɾ ą ⁘ ⌡ PLL	
₹ ˉ ʐ		PCB LVCMOS	
		PCB LVDS	
		PCB LP-HCSL	



~ ǎ	MHz	ų KHz	ų KHz

9.

ح Ð ч 6.00 mm × 6.00 mm × 0.60 mmMAX ح Ð ч QFN48 Й

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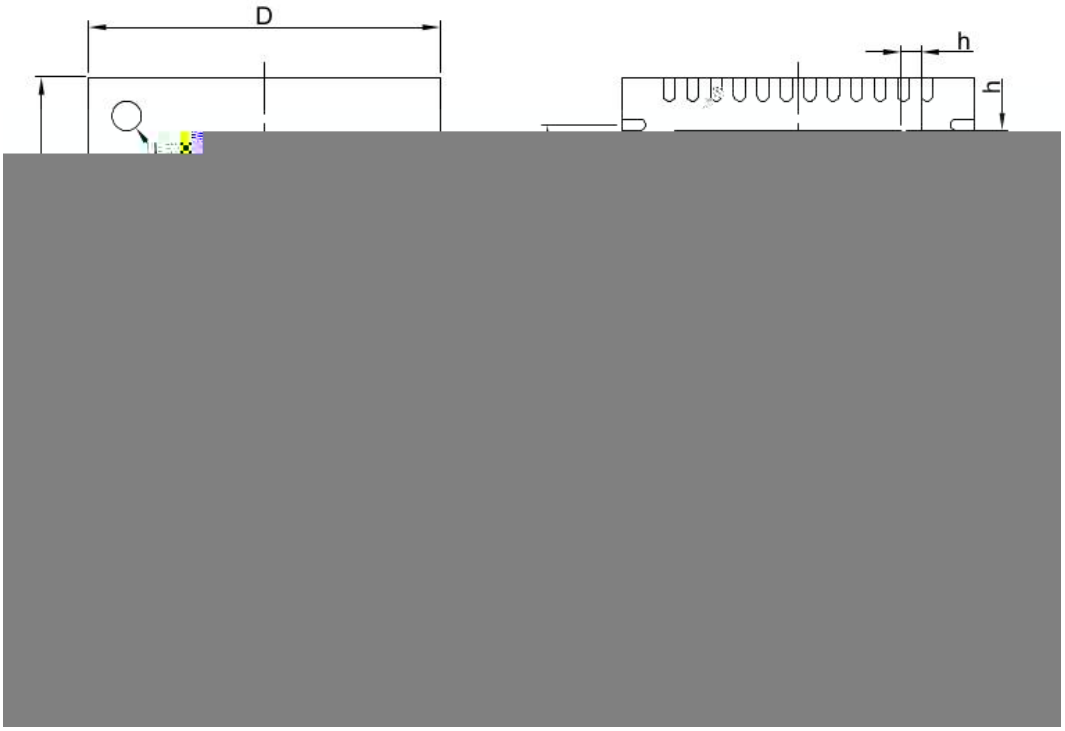

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	MIN	NOM	MAX		MIN	NOM	MAX
A	0.50	0.55	0.60	b	0.15	0.20	0.25
A1	—	0.02	0.05	c	0.12	0.15	0.18
D	5.90	6.00	6.10	h	0.30	0.35	0.40
D1	4.10	4.20	4.30	e	-	0.40	-
E	5.90	6.00	6.10	Ne	-	4.40	-
E1	4.10	4.20	4.30	Nd	-	4.40	-
L	0.35	0.40	0.45				

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10.

a β •

b “LS8T41505-A” A -i -H

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11. Ḥ

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LS8T41505		0 ~+70
LS8T41505-i		-40 ~+85
LS8T41505-H		-40 ~+105

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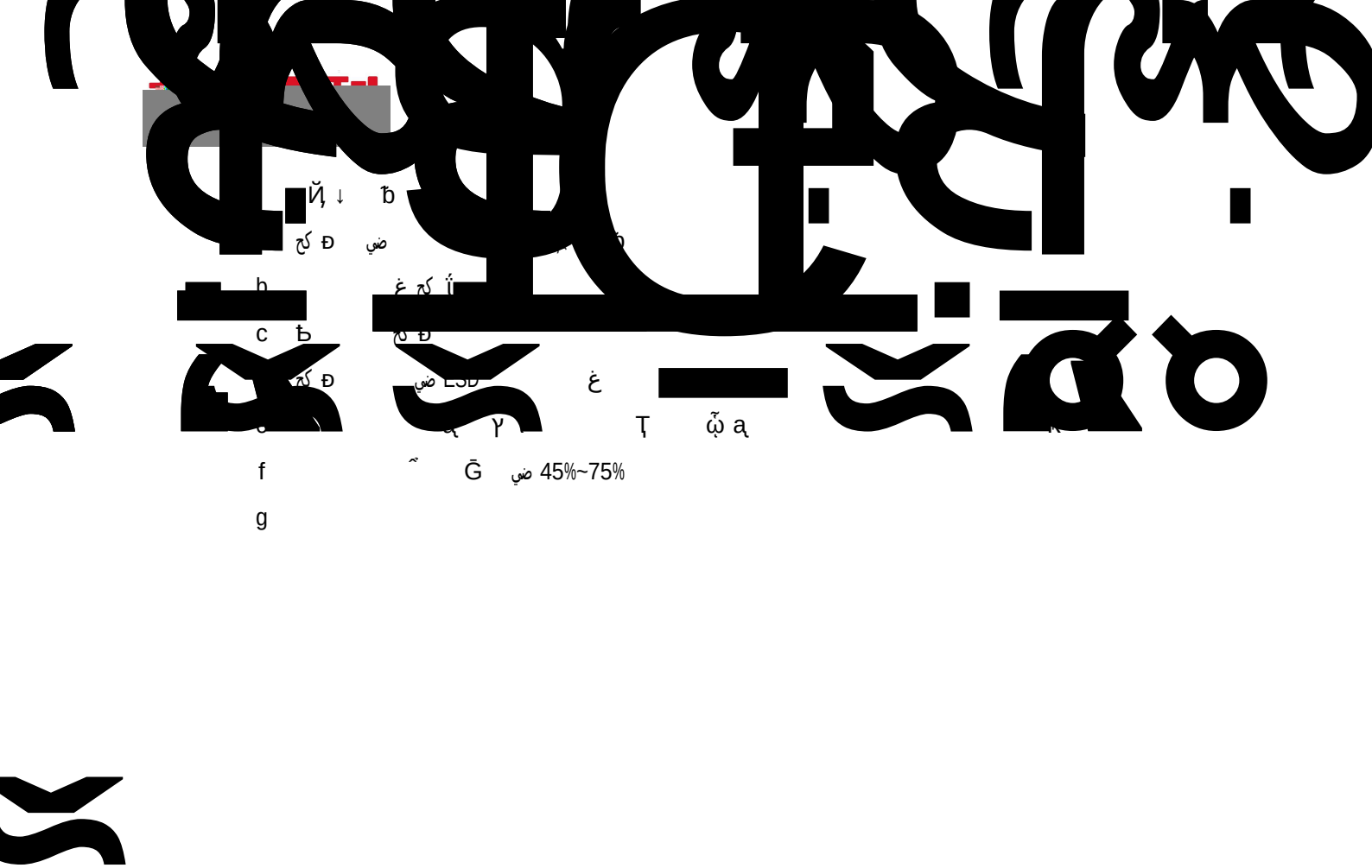
Й ↓ ƀ
ضي Ð كج
غ كج أ h
Ð ك c ƀ
ضي LSD Ð كج
ع
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ضي 45%~75% Ḡ
g

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EPAD 4.5mm SQ